Amendments To The Claims

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1. (**currently amended**) A DLL (Delay Lock Loop) circuit which synchronizes an external input clock applied from an outside of a system with an internal input clock used inside the system using a divider unit, the DLL circuit comprising:

a detection unit for detecting whether a pulse width of the external input clock is narrower **or wider** than a reference set value;

wherein the divider unit outputs a first divided signal ~~if~~ **when** it is detected that the pulse width of the external input clock is wider than the reference set value, and outputs a second divided signal ~~if~~ **when** it is detected that the pulse width of the external input clock is shorter than the reference set value.

2. (original) The DLL circuit as claimed in claim 1, wherein a pulse width of the first divided signal is narrower than a pulse width of the second divided signal.

3. (**currently amended**) A DLL (Delay Lock Loop) circuit which synchronizes an external input clock applied from an outside of a system with an internal input clock used inside the system, the DLL circuit comprising:

a buffer means for receiving and buffering the external input clock;

a detection means for detecting whether a period of an output signal of the buffer means exceeds a first delay time; and

a divider means for receiving the output signal of the buffer means and an output signal of the detection means and dividing frequencies of the output signals;

wherein ~~if~~ **when** the period of the output signal of the buffer means exceeds the first delay time, the detection means outputs a first logic level, and the divider means outputs a signal having a frequency obtained by dividing the frequency of the output signal of the buffer means into $1/2^M$ (where, M is an integer); and

wherein ~~if~~ **when** the period of the output signal of the buffer means does not exceed the first delay time, the detection means outputs a second logic level, and the divider means outputs a signal having a frequency obtained by dividing the frequency of the output signal of the buffer means into $1/2^{M+1}$.

4. (original) The DLL circuit as claimed in claim 3, wherein the first delay time is determined in consideration of a time taken from an input of the external input clock to an output of data from the system which uses the DLL circuit under the control of the DLL circuit.

5. (original) The DLL circuit as claimed in claim 3, wherein the external input clock and the output signal of the buffer means have the same period and the same duty rate, and the duty rate is 50%; and

wherein the detection means uses a high-level pulse width of the output signal of the buffer means in order to detect whether the period of the output signal of the buffer means exceeds the first delay time.

6. (original) A DLL (Delay Lock Loop) circuit comprising:

a clock buffer for receiving an external clock signal;

a first delay unit for receiving an output signal of the clock buffer;

a clock divider for dividing the output signal of the clock buffer;

a second delay unit for delaying an output signal of the clock divider for a predetermined time;

a third delay unit for delaying an output signal of the second delay unit;

a phase comparator for comparing a phase of an output signal of the third delay unit with a phase of the output signal of the clock divider;

a delay controller for receiving an output signal of the phase comparator and controlling delay operations of the first delay unit and the second delay unit;

a clock signal line for receiving an output signal of the first delay unit and controlling a data output of a data output buffer; and

a clock pulse width detector for receiving the output signal of the clock buffer and detecting a pulse width of the clock signal;

wherein the signal outputted from the clock divider under the control of an output signal of the clock pulse width detector has different divided states.

7. (**currently amended**) The DLL circuit as claimed in claim 6,

wherein ~~if~~ **when** the period of the output signal of the clock buffer exceeds a first delay time, the clock pulse width detector outputs a first logic level, and the clock divider outputs a signal having a frequency obtained by dividing the frequency of the output signal of the clock buffer into $1/2^M$ (where, M is an integer); and

wherein ~~if~~ **when** the period of the output signal of the clock buffer does not

exceed the first delay time, the clock pulse width detector outputs a second logic level, and the clock divider outputs a signal having a frequency obtained by dividing the frequency of the output signal of the clock buffer into $1/2^{M+1}$.

8. (original) The DLL circuit as claimed in claim 7, wherein the first delay time is determined in consideration of a time taken from an input of the external input clock to an output of data from the system which uses the DLL circuit under the control of the DLL circuit.